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Comparative Study of Noise Tolerant Techniques for Digital Circuits

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Abstract— *Nowadays, Domino logic methodology is widely used in design of high speed digital circuits and Technology has been scaled down to sub micron and deep sub micron level to achieve low power dissipation, less area. But circuit becomes more sensitive to noise. Though, dynamic logic circuits are natively is less noise tolerant. This dispute inclined to relentless with advancing technology scaling into nanometer process, especially created by the charge sharing, the sub threshold leakage current and crosstalk noise. We drift to yield some domino circuit topologies to raise the strength, lower the power consumption, raising the speed and increasing the noise immunity. To make design noise tolerant, so many techniques has been proposed and research is still going on in this area and needs more focus on this area. In this work, A different-2 noise tolerant techniques such as CONDITIONAL KEEPER DESIGN(CKP), FEEDBACK KEEPER(FKP), NOISE TOLERANT DYNAMIC LOGIC DESIGN (NTDL) are simulated at 90 nm technology at power supply of 5V with the help of TANNER EDA tool.*

Keywords: *Domino Logic circuit, domino logic with keeper, Sub micron, Noise tolerant.*

1. INTRODUCTION

Dynamic logic have a massive number of benefits such as lesser no of transistors, low power, higher speed as compared to static logic. In dynamic logic CMOS gate the switching threshold voltage is the transistor threshold voltage that is V_t but in static CMOS logic gate it is mainly around half the supply voltage. Hence, dynamic logic gates natively have less noise immunity than static logic CMOS gate. Input logic are regularly adapted to the NMOS Pull down network this makes dynamic circuits nearly 2 to 3 times faster. Because of higher thresholds, twice loading makes static logic slower. Dynamic logic uses only fast N transistors while static logic normally uses slow P transistors.

1.1. Effect of Technology Scaling

Technology has been scaled down to sub micron and deep micron level. Power supply has also scaled down. The threshold voltage has been scaled down to reduce the degradation in speed and maintain the dynamic power consumption within acceptable levels. But the threshold voltage results in:

- Quadratic reduction in dynamic switching energy
- Degradation in circuit speed due to reduced transistors current.
- Degradation in noise immunity of domino logic gate.
- Increase in sub threshold leakage current exponentially.

1.2. Effect of Noise in Deep sub micron

At the deep sub micron level three types of noise are present:

Charge sharing noise - It is caused by charge redistribution between the dynamic node and the internal nodes of the pull down network.

Leakage noise - It refers to the possible charge loss in the evaluation phase due to sub-threshold leakage current.

Coupling noise - Noise caused by the coupling effect, among adjacent signal wires.

1.3. Prevalent Techniques to Improve Noise tolerance

In the past two decades, no of circuit techniques have been developed with the view to improve noise immunity of dynamic CMOS logic gates. Classification of techniques based on their principle of operation:

Using keeper

Pre charging internal nodes

Raising source voltage

Loading input terminals of PDN

High Performance Noise Tolerant circuit techniques for CMOS dynamic logic.

1.4. Using Keeper Techniques

Keeper is a weak transistor employed at the dynamic node. The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. The use of keeper causes contention when the pull-down network is ON during the evaluation phase, resulting in slower overall gate performance. In wide fan-in gates, designed using very deep submicron process technology, the large leakage current through the n-network necessitates a very strong keeper to

retain the voltage at the dynamic node. There can be two types of keeper circuits:

Weak- always-on keeper

Feedback keeper

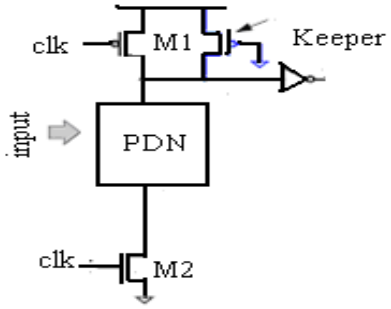

Fig. 1: Weak-always-on keeper

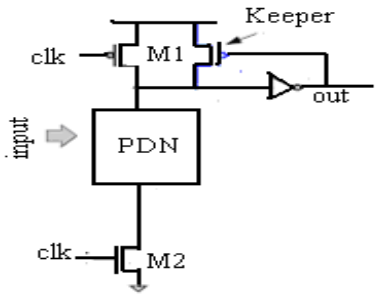

Fig. 2: Feedback keeper

In weak always on keeper the gate of the PMOS keeper is tied to the ground. Therefore, the keeper is always on. Feedback keepers are more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gate.

1.4.1 Conditional Keeper Design

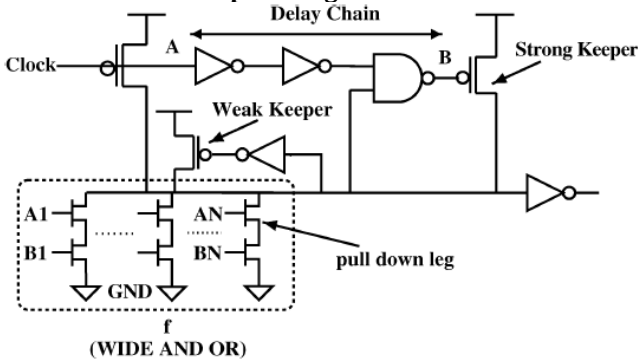

Fig. 3: Conditional Keeper Design

A weak keeper holds the state of the dynamic node during the transition window (when NMOS logic pulls down) and a strong keeper is conditionally activated based on the state of the dynamic node after a certain delay.

The weak keeper during the transition window results in reduced contention and a faster output transition, while the strong keeper during the rest of evaluation time results in good robustness to leakage and noise.

This technique has some limitations:

Significant amount of power dissipated in the inverter chain and the NAND gate that are used to generate the delay.

Delay of inverter chain is maintained for the worst case fNsP corner. The shorter delay time set for the fNsP corner degrades the performance of the dynamic gate in the sNfP corner.[14]

1.5. High Performance Noise Tolerant Circuits for CMOS Dynamic Logic

The logic function is implemented by means of an NMOS-based PUN, which aims to charge the node C according to the input signals. The transistor MY, MX, MK2 and the final static inverter act in a footless domino fashion. The node D works as a "virtual dynamic node"[16]

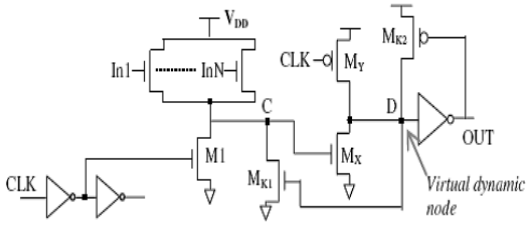

Fig. 4: Noise Tolerant Dynamic Logic Design

1.6. Pre charging Internal Node

Charge sharing between the dynamic node and the internal nodes in the pull-down network often results in false gate switching. To prevent the charge sharing problem, internal nodes in the pull-down network are precharged along with precharging the dynamic node.

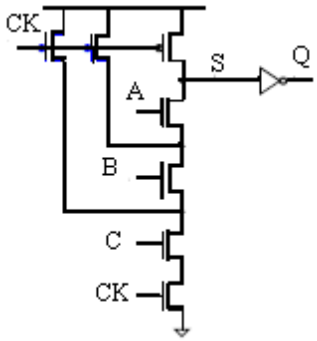

Fig. 5: Pre charging inernal node

When all internal nodes are precharged, this technique is able to eliminate the charge sharing problem at the cost of using a

large number of precharge transistors and the increased load capacitance on the clock net. Partial precharge design provides a tradeoff between noise immunity and overheads in chip area and in clock load. NMOS transistors can also be used to precharge the internal nodes.

Limitation**:** Precharging internal nodes alone is not very effective against external noises.

1.7. Raising Source Potential

It improves noise tolerance against both internal and external noises. Higher source voltage directly leads to increased gate turn-on voltage as the gate voltage has to be greater than the sum of the source voltage and the transistor threshold voltage when a transistor is turned on. Furthermore, due to the body effect, transistor threshold voltage is increased when the source voltage rises. This also contributes to improving gate turn-on voltage. PMOS Pull Up, NMOS Pull Up, Mirror Technique and Twin Transistor Technique are the major techniques based upon this strategy.[17]

It employs a PMOS transistor at node N2 forming a resistive voltage divider with the bottom clock controlled transistor. The voltage at node N2, which determines the switching threshold voltage of the dynamic logic gate, can be adjusted by changing the relative size of the PMOS pull-up transistor.[17]

Limitation**:** DC power consumption in the resistive voltage divider.

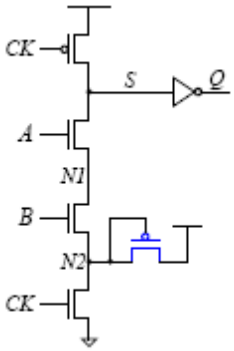

Fig. 6: Raising Source potential:PMOS Pull up

The gate of the pull-up transistor is connected to the dynamic node of the domino gate. This design allows the pull-up transistor to be shut off when the voltage of the dynamic node goes low; therefore, the dynamic node S undergoes rail-to-rail voltage swing. Also, the DC power consumption problem is partially solved. It occurs only under certain input combinations that do not turn on the pull-down network.[17]

Limitation: Problem of DC power consumption persists partially.

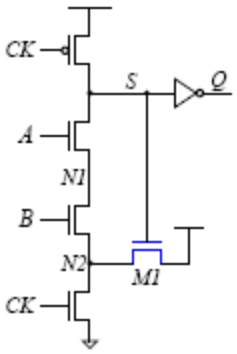

Fig. 7: Raising Source Potential: NMOS Pull up

2. RESULT AND SIMULATION

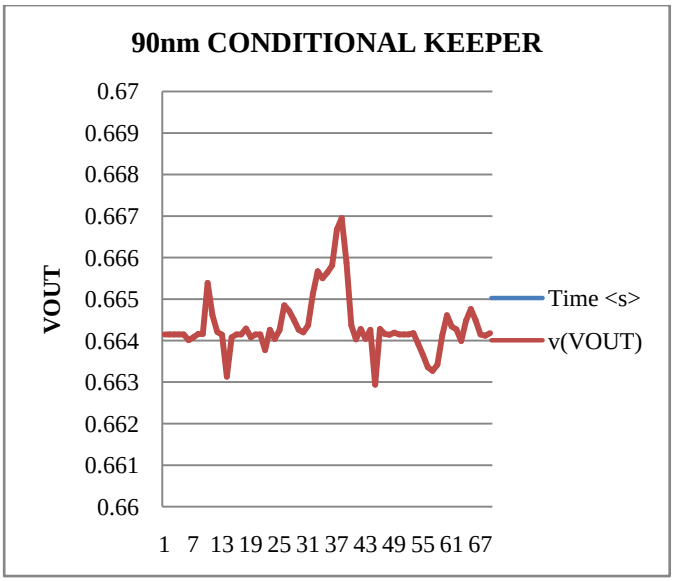

Fig. 1: Conditional Keeper Design

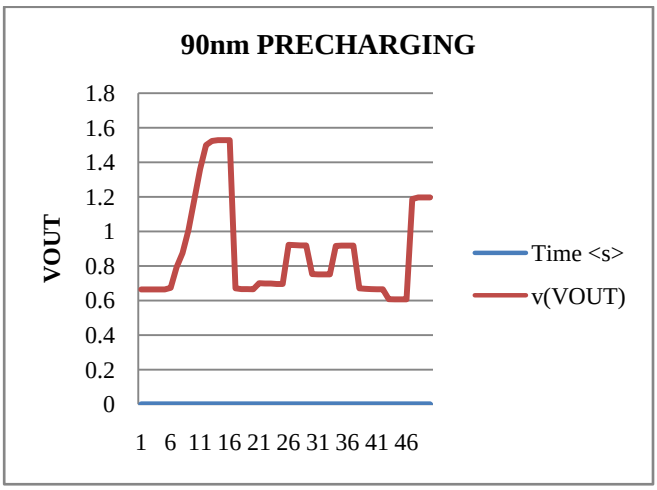

Fig. 2: Pre charging internal node

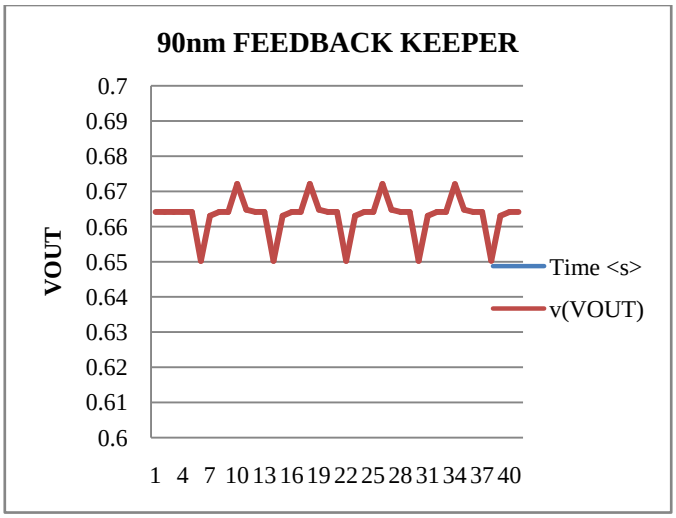

Fig. 3: feedback keeper

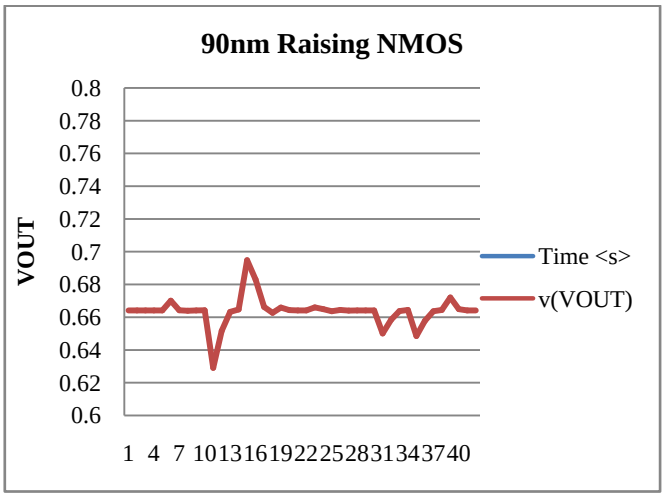

Fig. 4: Raising Source Potential: NMOS Pull up

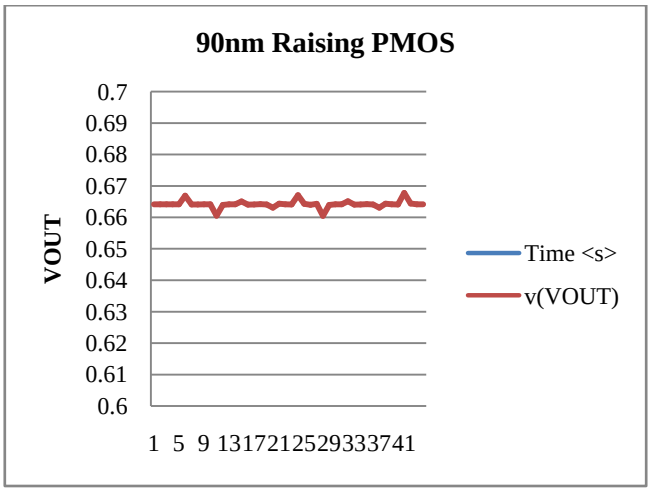

Fig. 5: Raising Source potential:PMOS Pull up

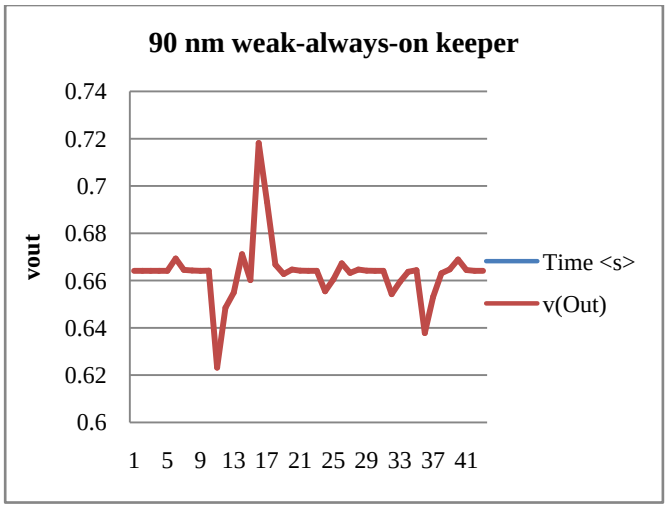

Fig. 6: weak-always-on keeper

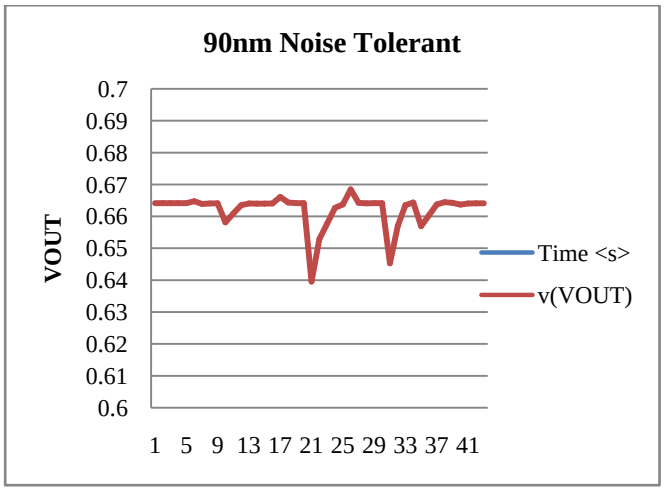

Fig. 7: Noise Tolerant Dynamic Logic Design

3. CONCLUSION

Under low power conditions, the deep sub micron dynamic circuits operating are more prone to noise. In deep sub micron low power dynamic circuits Conditional Clocking, Delayed Clocking , FTL with reduced charge sharing noise and FTL with increased input noise tolerance techniques are proposed to improve the noise immunity. These techniques gives promising results as far as noise tolerance is concerned but the research should focus on other dominant effects at sub-micron such as process variation along with noise tolerance in dynamic CMOS design.

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